In-circuit Testing of Low Voltage Devices

Technical Paper

Chris Jacobsen, Tony Saye, Ken Parker
Agilent Technologies, Inc.
Loveland, Colorado

Agilent Technologies

Introduction

In-circuit testing has been recognized as a valuable tool in electronics manufacturing for many years. The techniques used to test today's digital IC's are generally the same ones used since the first in-circuit test systems. Certainly device complexity has changed greatly over the years, but fundamentally, an in-circuit test of a digital device relies on a test system's drivers and receivers to stimulate and observe the device under test. Key to that is the ability for a test system to electrically isolate the device under test from the rest of the circuit. This is accomplished by either disabling the surrounding devices, or by "backdriving" devices that cannot be disabled.

What has been changing over the years is that more of today's devices operate at an increasingly smaller supply voltage. This is necessitated by the drive towards smaller, faster, and power conserving devices. In general, "low voltage" devices use a supply of 3.3V or less. "Ultra-low voltage" devices use a supply of 1.8V or less. While supply voltages shrink, the test system's drivers and receivers must accommodate the resulting lower thresholds and smaller margins, while continuing to maintain accuracy.

In-circuit testing of digital devices

Historically, in-circuit testing of digital devices brought about two primary concerns:

1) Signal integrity – the test system's ability to drive and receive signals resulting in a reliable test of the device.

2) Safe digital isolation – the test system's ability to ensure the device under test is digitally isolated from the rest of the circuit without causing damage to any of the devices in the circuit.

With low-voltage devices, these concerns have not changed. First, with the smaller operating voltages, the test system must be capable of maintaining the appropriate signal integrity needed for a reliable test of the device. Second, with advances in device technology, the test system must continue to ensure safe digital isolation of the device under test.

Signal integrity

The most obvious component of signal integrity during in-circuit test is driver and receiver accuracy – the test system's ability to drive and receive signals within the proper margins. As mentioned, this presents additional challenge due to the smaller low-voltage parameters. However, there is more to in-circuit signal integrity than a tester's driver and receiver specifications. We will also need to consider driver impedance, tester to fixture interface, fixture design, fixture to board interface, etc.

Specific characteristics of signal quality are voltage over and undershoot. If not designed properly, an in-circuit test can contribute to voltage over and undershoot. This presents both test reliability and a device safety issue. Moderate amounts of voltage over or undershoot can cause test stability issues – false failures (a good part is called bad) or escapes (a bad part called good). Voltage over or undershoot in excess of device maximums can cause device damage.

Safe digital isolation

During digital isolation and test of an IC, potential damage to the device under test as well as other devices in the circuit remains a concern.

The primary mechanisms for device damage during in-circuit test are backdriving and voltage overshoot and undershoot.

When an upstream device cannot be disabled, we need to backdrive the upstream device to ensure the correct logic level is received at the device under test. With DFT (Design for Test) placing more emphasis on device disabling, backdriving should be less of a concern. However, there continue to be cases where backdriving is utilized during the course of modern in-circuit testing. Since the days of the 3065, Agilent has used Safeguard to automatically evaluate and inhibit testing of devices that may cause backdriving damage. The Safeguard In-circuit method is backed with research and offers a predictive method to ensure device safety. Recently, this research has been updated to include today's low-voltage logic families. This research is described in the second half of this paper.

Implications of low-voltage at in-circuit test

What is low voltage

Since the initial introduction in 1989, the Agilent 3070 in-circuit test system provides a complete solution for testing low-voltage logic devices both safely and accurately. Capabilities such as "per pin" voltage programmability with typical accuracy of 50mV, Safeguard, Boundary Scan, and short-wire fixture technology provide the most versatile, industry leading solution available today. Agilent Medalist 3070 and i5000 customers are successfully testing low-voltage logic down to 1.2V. The following describes the issues and solutions for low-voltage logic testing.

The newer device technology that In-Circuit test systems are being asked to address is migrating towards low-voltage logic below 3.3 volts. The market for low-voltage logic devices includes battery-powered devices like PDA's and MP3 players. In addition, the lower power dissipated by these devices are finding use in computers and communication boards. The lower supply voltages also allow sub-0.6 micron semiconductor manufacturing processes to allow denser and more complex designs.

As mentioned earlier, low-voltage logic devices have a supply voltage of 3.3V or less. Ultra low-voltage logic has a supply voltage of 1.8V or less. The lowest supply voltage for ultra low-voltage devices seen to date is 0.8V. It is expected that broad use of ultra-low voltage will not be seen for another 3-4 years.

Typical low-voltage logic levels

Figure 1 shows the relative voltages for various logic families. Note that V_{oh} and V_{ol} correspond to the tester's receiver thresholds (i.e., a receiver's high threshold should be set below the V_{oh} voltage while a receiver's low threshold should be set above the V_{ol} voltage). Likewise, the V_{ih} and V_{il} correspond to the tester's driver voltages (i.e., the driver high voltage should set above V_{ih} and the driver's low voltage should be set below V_{il}). Note that as the supply voltage decreases, the margins for the tester's drive and receive voltages become smaller.

Low-voltage standard specifications

Table 1 below lists the logic levels for various supply voltages down to 1 V as described in the respective JEDEC publications [2]. Note that with the lower voltage ranges, the input and output thresholds are a function of the actual supply rather than a fixed voltage level. Not only are the margins getting smaller, but the margins can shift slightly with changes in supply.

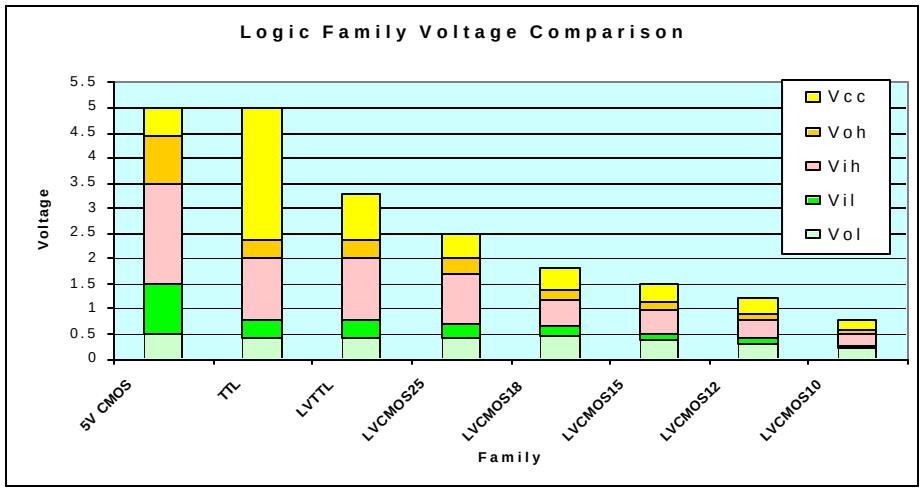

Figure 1 Logic Family Voltage Comparisons

JEDEC Standard [2]	Family	Nom. Supply	V_{DD}	V_{IH}		V_L		V_{OH}	V_{OL}
				Min	Max	Min	Max	Min	Max
No. 8-5		2.5 V	2.5 ± 0.2	1.7	V_{DD} + 0.3	-0.3	0.7	1.7	0.7
No. 8-6	HSTL	V_{DDQ}	V_{REF}	V_{REF} + 0.1	V_{DDQ} + 0.3	-0.3	V_{REF} - 0.1	V_{DDQ} - 0.4	0.4
		1.4 – 1.6	0.68 – 0.90						
No. 8-7		1.8 V	1.65 – 1.95	0.65 V_{DD}	V_{DD} + 0.3	-0.3	0.35 V_{DD}	V_{DD} - 0.45	0.45
No. 8-B	LVTTL	3.3 V	3.0 – 3.6	2	V_{DD} + 0.3	-0.3	0.8	2.4	0.4
	LVCMOS	3.0 V	2.7 – 3.6	2	V_{DD} + 0.3	-0.3	0.8	V_{DD} - 0.2	0.2
No. 8-11		1.5 V	1.4 – 1.6	0.65 V_{DD}	V_{DD} + 0.3	-0.3	0.35 V_{DD}	0.75 V_{DD}	0.25V_{DD}
No. 8-12		1.2 V	1.1 – 1.3	0.65 V_{DD}	V_{DD} + 0.3	-0.3	0.35 V_{DD}	0.75 V_{DD}	0.25V_{DD}
No. 8-14		1.0 V	0.9 – 1.1	0.65 V_{DD}	V_{DD} + 0.2	-0.2	0.35 V_{DD}	0.75 V_{DD}	0.25V_{DD}

Table 1 Low-voltage specifications

Challenges with low-voltage in-circuit testing

Low-voltage logic can be problematic to test on in-circuit test systems for a variety of reasons:

- The low voltage required for driving a logic '1' or '0' could be difficult to achieve due to driver inaccuracies.
- The low voltages driven by the logic device on the DUT require high accuracy receivers on the test system to properly differentiate between a logic '1' and '0'.
- High driver impedance in the path can cause the output voltage that appears at the DUT to be lower that the V_{ih} for that device due to an IR voltage drop across the drive path. This would occur during a backdrive situation but not when the upstream device is in a high-impedance state.
- The low voltages involved with testing low-voltage logic devices mean that noise seen at the DUT, including fixture effects, becomes a more significant factor in test stability.
- Low-voltage devices mean lower maximum voltage on device pins. Exceeding these maximum ratings can damage the device under test (e.g., gate oxide breakdown). In-circuit test systems designed with "per-channel" programmability, like the Agilent Medalist 3070 and i5000, can help minimize exceeding device ratings, especially in a mixed-voltage device or design.

Successful low-voltage testing

For repeatable testing of low-voltage logic, you must be concerned not only with the test system specifications, but also with the DUT characteristics and fixture effects. No matter the logic used, good test and fixture design is paramount to successful, reliable, and repeatable testing. With low-voltage logic's smaller margins, good test and fixture design become more critical. With this in mind, low-voltage logic devices can certainly be tested on the Agilent Medalist 3070 and i5000 systems. Here are some tips to help ensure success testing low-voltage logic on the Agilent 3070 and Agilent Medalist i5000:

- The Agilent Medalist 3070 and i5000 typical specifications are much better than the "guaranteed" specs (± 50mV for drivers, ± 30mV for receivers, typical).
- Set the drive and receive levels to work within the accuracy specifications of the drivers and receivers.
- Make sure to define the appropriate logic families in the 'board' file and reference them in the low-voltage logic libraries (check the 'family' statement in the VCL library).
- Disable or condition upstream devices to minimize backdrive current. This will reduce the inaccuracy caused by the voltage drop due to the output impedance of the driver and other fixture-related impedances. The Agilent test system not only provides for disabling and conditioning of immediate upstream devices, but also allows multiple level disabling and conditioning to reach devices upstream of the upstream devices.
- Use a ground plane with a short-wire fixture or a "wireless" fixture technology to minimize noise that can cause intermittent tests. Avoid long-wire fixtures as these tend to pick-up more electrical noise. A ground plane can also reduce the effects of "ground bounce" in the test fixture.
- For multiplexed testers like the 3070, set slew rates carefully to minimize overshoot and undershoot while still meeting the minimum slew rate of the device. In a worst case situation (high amount of back-drive current), additional fixture electronics in the form of ferrite beads or protection diodes may be required to prevent damage to the device under test.
- Advanced unmultiplexed testers like the Medalist i5000 have a much cleaner path from the driver to the DUT. Rather than the typically slew rate

specification, the Medalist i5000 driver has a fixed rise (and fall) time of 12nS for the driver to go from 0V and the drive high voltage. Because the i5000 is unmultiplexed, the path from driver output to interface pin doesn't have any stubs going off to other relays and minimal capacitive loading. Furthermore, since the drive paths are much more consistent on the i5000, it is possible to design the drivers for "rounded" corners on their edges. This lowers the frequency content of the edge resulting in less ringing. By controlling the frequency content in this way, the speed of transition through the logic threshold can be maintained without the need to minimize the slew rate. This results in a signal that contains less overshoot and ringing for low-voltage signals without compromising on slew rates.

- In very noisy environments, use twisted-pair wires for the ultra-low-voltage signals in the short-wire fixture. Also, use decoupling capacitors to minimize the noise seen by the DUT.
- Be diligent with fixture maintenance to minimize probe contact resistance. Any unnecessary impedance in the signal path can cause inaccuracies with the drive voltage at the DUT, especially during backdriving.

Driver accuracy

Driver accuracy is how accurately the pin electronics driver generates the specified drive voltage to the DUT. Usually this is specified at the tester interface pin as there are factors that affect the voltage at the DUT. A driver is more accurate when the driver accuracy specification is lower. The Agilent Medalist 3070 and i5000 have a guaranteed driver accuracy of ± 100mV. This means that if you program the system to drive a particular voltage, the voltage measured at the test system interface is within 100mV of what you programmed that voltage to. For example, if you instruct the 3070 to drive a voltage to 3.0V, the voltage appearing at the tester interface will be between 2.9V and 3.1V (see Figure 2). Compared to the guaranteed driver accuracy, the typical Medalist 3070 and i5000 driver accuracy is much better. In particular, in the “ultra low-voltage” logic range (0.25V-1.5V), the Agilent 3070 and Medalist i5000 driver accuracy is better than ± 50mV.

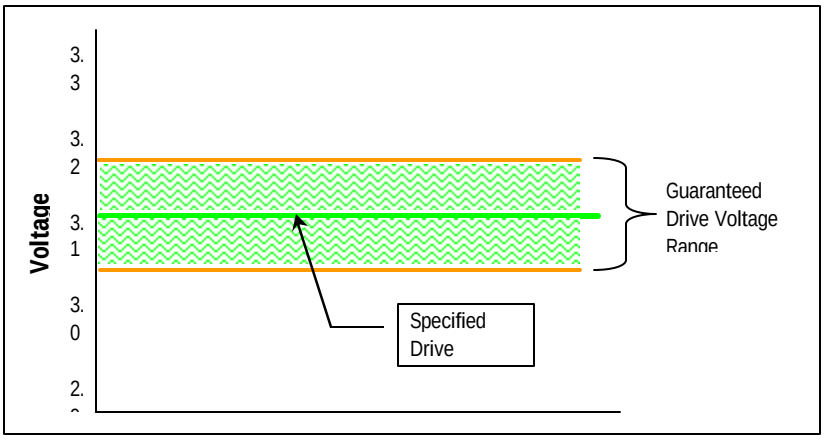

Figure 2 Driver voltage range (± 100mV accuracy)

Receiver accuracy

Receiver accuracy refers to how accurately the comparator on the receiver of the pin electronics responds to a specified threshold level. The receiver accuracy also is dependant upon the accuracy of the circuitry used to generate this reference voltage. Again, the receiver is more accurate when the receiver accuracy specification is lower. The Agilent 3070 and Medalist i5000 has a guaranteed receiver accuracy of ± 100mV. However, the typical receiver accuracy is on the order of ± 30mV! Since the Agilent 3070 has a dual threshold receiver, both of these thresholds are tied to the receiver accuracy. The Medalist i5000 has a single threshold receiver.

For example, if you specified that the receive high threshold was 2.5V, it is possible that a voltage seen by the receiver that is above 2.4V is considered a high while a voltage below 2.6 could be considered not a high (see Figure 3).

Likewise, if you set the receive low threshold to 0.5V, it is possible that a

voltage lower than 0.6 is considered a low while a voltage above 0.4V is considered not a low. If the 3070 VCL test is expecting a logic '1' on the receiver, then the received voltage must be above the receive high threshold. Likewise, if the test is expecting a logic '0' on the receiver, the received voltage must be below the receive low threshold.

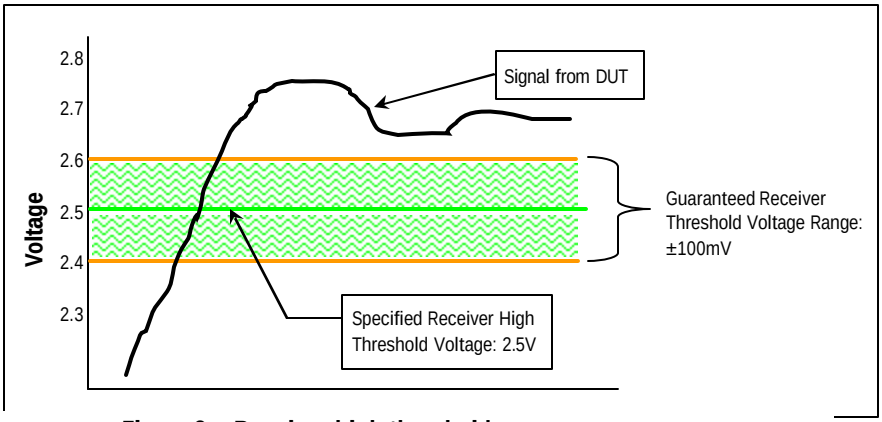

Figure 3 Receiver high threshold range

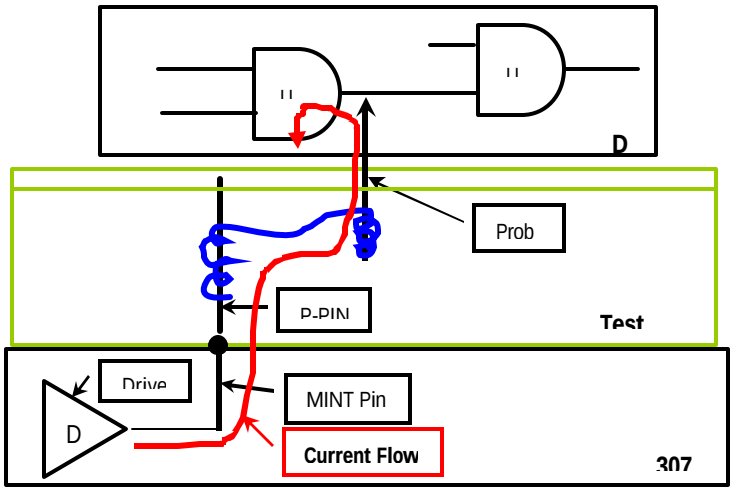

Figure 4 Current flow from the driver during backdriving

Driver output impedance

The voltage at the DUT depends on the driver's output impedance at a given current level. This current flow is usually the result of backdriving an upstream device. If the driver is not driving a high impedance load, then the amount of current flowing to force the node to the desired logic level could be significant. To minimize the corresponding voltage drop, the output impedance of the driver should be as small as possible. The output impedance is a combination of the actual output driver electronics impedance plus the resistance of the signal path to the tester interface pins.

Figure 4 shows the flow of current when testing a logic device on the DUT. The current flows from the driver through its characteristic output impedance, through the Module Interface Pin (MINT pin), which makes contact with the personality pin of the ICT test fixture, through the wire-wrap wire to the probe socket, up through the test probe, which makes contact with the test pad on the DUT, and finally through the device the driver is trying to backdrive (in this case, the output stage of device U1). For example, the Agilent 3070 specifies the output impedance at the tester interface pins to be somewhere between 1.15 and 2.0 ohms at 500mA of current supplied by the driver. With this amount of current, there will be somewhere between 575mV and 1V drop in the voltage applied at the device under test compared to what the driver was programmed to supply. This becomes very significant for low voltage logic devices since the supply voltage could be 1.8V or less. Note that the Agilent Medalist i5000 system has a driver output impedance of 0.87 ohms, typical. At 500mA, this would result is a 435mV voltage drop.

Fixture voltage drop during backdrive conditions

Once the signal leaves the relatively controlled impedance of the tester electronics, it must pass through the test fixture wiring and test probes to get to the DUT. Each of these components has impedance associated with it that can have an adverse effect on the driver voltage as seen at the DUT. For example, Figure 5 shows the various impedances in the drive path of the tester-generated signal to get to the device under test. There is the impedance from the tester to the test fixture (Z_{ppin}), the impedance

of the fixture wire (Z_{wire}), the impedance of the probe to the DUT (Z_{probe}) and the load at the DUT itself (Z_{load}) in addition to the output impedance of the driver (Z_{out}).

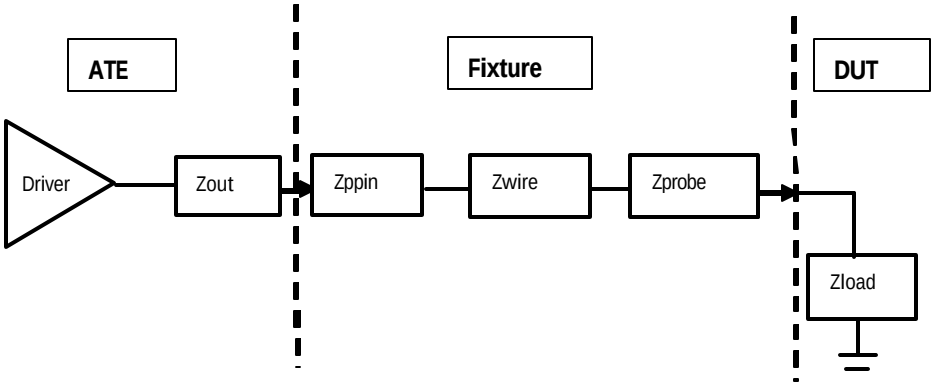

Figure 5 Impedances during digital testing

We already know that the output impedance of the Agilent 3070 test system driver, for example, is between 1.15 and 2 ohms, and it is not uncommon to have some resistance in the test fixture wiring (Zppin + Zwire + Zprobe). Therefore, we could have somewhere between 1 and 3 ohms impedance before we get to the DUT. At 100mA, we would see a drop of about 100mV to 300mV before it gets to the DUT. This may not seem like much when testing TTL where the drive high level should be about 3.5V and the TTL device expects a high on its input to be above 2.0V. The voltage drop in our example would supply a voltage of about 3.1V to the DUT.

However, if we have a low-voltage device running at 1.5V, the input high voltage (minimum) is about .98V. If driving 1.3V with a 300mV drop (100mA through 3 ohms worst case), the actual voltage at the DUT will be very close to the minimum for a drive high input to the LV device.

Reducing fixture voltage drop

The potential voltage drop through the fixture impedances can be minimized by:

- Minimizing the backdrive current. Disabling upstream devices is the most effective way to minimize backdrive current. If a device cannot be disabled, then 'conditioning' the upstream device to a known fixed output can still help minimize backdrive current. In general, it takes less current to overdrive a device output that is at a logic '1' to a logic '0' than it does to overdrive an output that is at a logic '0' to a logic '1'. Both the Agilent Medalist 3070 and i5000 support multiple-level upstream disabling and conditioning along with multi-vector disabling.
- Minimizing the fixture impedance. Begin with good fixture design and keep wire lengths as short as possible during fixture build. The Agilent Medalist 3070 and i5000 both support short-wire fixturing as the standard fixture technology. Furthermore, the non-multiplexed i5000 does not have the resource conflicts found in the 3070. This results in shorter wires in short wire (or wireless) fixtures.
- As fixtures get older, probes wear and get contaminated, increasing contact resistance. A fixture maintenance program has always been valuable, but increased diligence in fixture maintenance will help ensure test reliability.
- Increasing the drive voltage a small amount. Many ultra low-voltage devices are designed to work in mixed-voltage designs and are therefore tolerant of higher input voltages. However, when backdriving, it is not recommended to increase the voltage above Vcc. In fact, setting the maximum drive high voltage to Vcc-0.1V would prevent exceeding device ratings while accommodating the

100mV accuracy specification. In the case above, the drive voltage would then be 1.4V resulting in an adequate drive level even with the 300mV voltage drop.

Noise in the fixture

When dealing with low-voltage logic devices, system noise becomes a more significant factor to reliable testing. The noise appearing at the DUT input or test system receiver can affect the DUT operation or perceived response from the DUT. Most of the other issues that affect low-voltage logic testing can be compensated for or are controlled by the test system itself. Noise, however, can be generated by many sources; the test system, the DUT, electrical machinery located near the test system or sharing the power drop, and even the overhead lights. This is the main unknown when it comes to low-voltage testing. We must try to minimize noise in the test fixture as best as we can. In addition, being able to have more ground connections to the DUT will help with noise caused by high current transitions that you might see in Boundary Scan testing. The Medalist i5000 unmultiplexed architecture allows any pin to provide a ground, minimizing the effect. In addition, you can use a ground plane in the test fixture.

Programmable loads

Most ATE systems can connect pull-up or pull-down loads to the output of logic devices to pull the outputs to either a logic '0' or a logic '1'. However, these programmable loads can interfere with the operation of the device. If the pull-up load is connected to a voltage above Vcc for the device, damage to the chip can occur or the device will not function correctly. In these cases, specify no programmable load or place pull-up or pull-down resistors in the test fixture. The Agilent Medalist 3070 provides pull-up and pull-down loads implemented as a current source that is limited to the receive high and receive low voltages respectively. The Medalist i5000 uses fixed resistors tied to the drive high voltage level for pull-ups and 0 volts for the pull down.

DUT power supply accuracy

With low voltage logic devices comes the need to have the supply voltages to the board be much more accurate and regulated. Many times, the device manufacturer has specifications regarding the power supply output voltages. This is particularly true for PC motherboards and chipsets. Better regulation of the supply voltages is required to minimize noise and reduce intermittent tests. In addition, if your DUT draws significant current, pay close attention to the actual supply voltage at the DUT. The power supplies can incur voltage drop due to the supply current through the cabling and fixture wiring. In some cases, the voltage supplied to the board is converted to other voltages via on-board regulators (many PC motherboards use this technique). You must verify all these voltages are correct and meet the specifications for the logic devices on the board.

The DUT power supplies shipped with the Agilent board test systems are lab-grade supplies that provide high accuracy voltages to the DUT. The load regulation of the supply provides ± 1mV output change due to a change in load resistance on any output of the supply. Programming accuracy is ± 19mV + 0.06% of programmed value at voltages less than 23V. The Agilent Medalist 3070 and Agilent i5000 also do remote sensing of the supply outputs in the test fixture that can be connected to the DUT to ensure there is no drop in the supply voltage at the DUT.

Slew rate

For ultra-low-voltage logic, the differential between logic '0' and logic '1' is small (as low as 500mV). At 100V/uS (0.1V/nS) slew rate, it will take 5nS to slew through that range. Another way that some low voltage device manufacturers look at this specification is to invert the specification. 100V/uS is the same as 10nS/V. Some low voltage devices require a fast slew rate to avoid having the output oscillate which can cause additional noise in the system and possible damage to the device under test. Make sure you go as fast as you can with the slew rate to avoid oscillation but balance that with minimizing overshoot and undershoot of the signal.

Wire length continues to play a significant role in this aspect of signal quality as well. Utilizing the short-wire technique of the Agilent test

system will help ensure optimum signal integrity.

Safeguard In-circuit for low-voltage

Protecting devices from backdrive damage

Backdriving a digital device to force its output to the opposite logic level can potentially damage the output of that device. A predictive approach was introduced in 1985 [1] that limits the test execution time to those that are deemed safe by analysis. The analysis looks at a number of factors for a logic family including the backdrive current, maximum overdrive power, package type, thermal resistance of the junction-to-case, and nominal operating temperature of the die. It also looks at the board topology to determine which devices upstream from the device you are testing will be backdriven. It will then set the maximum safe backdrive time for the test. If the test execution time takes longer than the maximum safe backdrive time, the test will be "inhibited". The test system will not allow execution of an inhibited test without additional programmer action. A test programmer can modify the test in a number of ways to "uninhibit" the test, thus allowing it to be executed. The programmer can edit the test to place upstream devices into "tri-state" mode, adjust the vector cycle time so that it runs faster (less time), or break the test up into separate tests to minimize the backdrive time.

Since the algorithm was developed before low-voltage devices were developed, it may not be obvious that the algorithms are still valid with current devices. Key to the original technique was in-depth research conducted on devices within the logic families in existence at that time. This research was the basis for the algorithms safe test time calculations.

Fortunately, research describing the failure mechanisms in modern integrated circuits continues. A recent JEDEC publication [2] defines failure mechanisms present in modern devices and provides models for these mechanisms. For in-circuit test, we are only interested in failure mechanisms that are activated by the in-circuit test environment, specifically by backdrive. Current research [3] continues to extend the predictive technique when used with modern low-voltage devices. The predictive and conservative nature of algorithm – disallowing inadvertent unsafe test execution – continues to offer advantage during in-circuit test of modern logic families.

IC degradation mechanisms and accelerators

In examining the effects of backdrive during an in-circuit test of an IC, the concern is not only with potential device failure, but also with device degradation. Device degradation is not an immediate device malfunction, but rather a reduction in the expected lifetime of a device. Mechanisms leading to device degradation have been researched with respect to the expected degradation as a result of backdrive during in-circuit test [1], [3]. For example, backdrive during a 1ms in-circuit test may cause a lifetime reduction on the order of seconds depending on the specific degradation mechanism. However, over the expected lifetime of a device (years), this lifetime reduction of a few seconds due to backdrive during in-circuit test would be considered insignificant.

According to [3], backdrive current itself does not present a danger to the device. This is because the amount of backdrive current is the same as the maximum amount of current present during normal logic transition. The same can be said for output voltage during backdrive. The voltage forced on the output is simply the value representing a normal logic "0" or logic "1". Likewise, power dissipation does not significantly exceed that in normal conditions. What really creates the potential for damage or degradation during in-circuit test is the amount of time these maximums are applied. During backdrive, the maximum voltage and current is applied for a significantly longer period of time compared to normal operation. The resulting power dissipated, over a longer period of time, means a greater rise in device temperature. With temperature as the most common accelerator of device degradation, we can see why understanding power dissipation, the resulting temperature rise,

and ultimately the duration of backdrive is important. The algorithm helps to protect devices by considering factors such as current, power dissipation, and temperature to predict the maximum safe test time for that given device under test. If the test is less than that safe test time, it will execute with no device failure or significant degradation expected. If the test time exceeds that safe test time, the test will not be allowed to execute without further programmer action.

It should be noted that there are a few qualifications to the above statement. First, voltage level maximums will not be exceeded by the voltage-forcing source (i.e. tester driver) only if the proper voltages can be selected. For example, a driver fixed at 3.5V will not be able to safely drive a device rated to 2V maximum. This is especially critical with low-voltage and mixed-voltage designs. Fortunately, selecting correct voltage levels is easy to accomplish with programmable drivers and receivers.

Second, any output change in state must be due only to the voltage-forcing source, not due to a change in the input. If an input change causes a change in the output state, over voltage can occur due to the inductance of the backdrive circuitry and/or the off chip interconnects [1,4]. This can lead to additional device stress, potentially exceeding device maximums and causing device damage. In an effort to avoid over voltage, it is recommended that we should backdrive a fixed output. Furthermore, since one state is typically easier to backdrive than the other, i.e. requires less current, we should select the fixed state that presents the least stress. Multiple level pre-conditioning of upstream devices accomplishes that goal.

Finally, the earlier statement assumes only one output is backdriven at a time. During the course of in-circuit testing, it is entirely reasonable to expect that multiple outputs will be backdriven simultaneously. Since power or ground will always carry backdrive current, we have to consider the sum of backdrive currents distributed across the power or ground bond wires. A conservative assumption would be to assume a single power and ground bond wire. This single bond wire carrying the sum of backdrive currents can exceed normal conditions not just over time, but also in absolute current. The algorithm also sets maximum acceptable current and temperature rise for a bond wire [1] based on the sum of the backdrive currents of the overdriven outputs. It should be noted that this would be worst-case since many devices typically have multiple power and ground bond wires. The algorithm continues to help protect against device failure and unacceptable degradation in mature devices as well as modern devices.

Degradation mechanisms relevant for in-circuit test

A number of device degradation mechanisms were researched [1] when the original Safeguard In-circuit algorithm was developed. The mechanisms then considered were: Second breakdown, Electromigration, Corrosion, Interaction with other materials, Intermetallic growth, Surface reconstruction, Dielectric breakdown, Surface charge accumulation, Charge injection, Thermal fatigue, CMOS latch-up, Source-drain punch through, SiO_2 breakdown, and Bond wire fusing.

The Hewlett-Packard product note [1] concluded that second breakdown, interaction with other materials, thermal fatigue, and SiO_2 breakdown are insignificant degradation mechanisms during in-circuit test. The recent JEDEC publication [2] draws that same conclusion for modern devices.

Surface charge accumulation in older devices could lead to some, but generally acceptable, device degradation [1]. CMOS latch-up and source-drain punch through were deemed insignificant in original research [1], with the qualification that CMOS latch-up is not a concern when the in-circuit test is properly designed. With more recent research [3], all three of these mechanisms – surface charge accumulation, CMOS latch-up, and source-drain punch through – have lost significance with the advances made in solid-state technology. Corrosion has also become a less significant factor in modern packaging [3]. With moisture and contamination as its accelerators, it is not

activated by in-circuit backdrive.

The most recent research [3] focuses on electromigration, time dependent dielectric breakdown, and bond wire fusing as significant degradation mechanisms relevant to in-circuit test. Hot-carrier injection is accelerated by a same-state condition across the output port – the situation exactly created by backdrive. As such, it is further evaluated in current research [3]. Finally, while not cited in [1], stress migration does receive consideration in [3].

Table 2 summarizes these degradation mechanisms of IC's in general. Included are comments regarding that particular mechanism's significance to device degradation caused by backdrive during in-circuit test.

Degradation expected during in-circuit test

As mentioned, only a subset of IC degradation mechanisms is relevant to in-circuit test. Those mechanisms identified earlier were specifically examined and remodeled to estimate their expected contribution to lifetime reduction.

Original research [1] indicated that electromigration would cause a lifetime reduction of no more than 966 ms as a result of a 1 ms test. For modern devices, backdriving for 1ms results in a lifetime reduction on the order of seconds to tens of seconds [3]. This small increase in degradation is still negligibly small relative to the expected lifetime of a device.

Stress migration, newly considered by [3], has an acceleration factor orders of magnitude smaller than for electromigration. Therefore, stress migration due to backdrive is not significant. Likewise, time dependent dielectric breakdown has an acceleration factor due to backdrive on the same order as stress migration. Hot-carrier injection also has a small acceleration factor. These mechanisms as well are not significant contributors to degradation during in-circuit test.

Degradation mechanism	Significance during ICT
Second breakdown	Continues to be insignificant
Interaction with other materials	Continues to be insignificant
Thermal fatigue	Continues to be insignificant
SiO_2 breakdown	Continues to be insignificant
Surface charge accumulation	Less significant with progress in solid-state technology
CMOS latch-up	Less significant with progress in solid-state technology
Source-drain punch through	Less significant with progress in solid-state technology
Corrosion	Less significant with moisture and contamination as its primary accelerators
Electromigration	Significant
Time dependent dielectric breakdown	Significant
Bond wire fusing	Significant
Hot-carrier injection	More significant since [1] published
Stress migration	Newly evaluated

Table 2 IC degradation mechanisms

For a single bond wire and a single backdriven driver, [3] found that with most logic, the bond wire fuse current was greater than the backdrive current. Only in BCT and F parts examined did the backdrive current exceed the fusing current with fusing times on the order of 40 ms to over 1.5 seconds depending on the specific part. Of course, during in-circuit test, it is common to backdrive multiple outputs at the same time. In this case, the sum of the backdrive currents should be used and distributed across the power or ground bond wires. Since it is typically not known or easy to determine the number of power and ground bond wires, a conservative assumption would be to assume only a single power and ground bond wire carries the sum of the currents of the overdriven outputs. The Safeguard models separately specify the amount of current needed to overdrive "0" and "1". With this, and through the device models and board topology, Safeguard In-circuit knows exactly how many outputs are overdriven and exactly how much current will be needed. This allows the algorithm to inhibit the test when current, temperature rise, or time restrictions are violated.

Finally, [3] provides an interesting conclusion regarding differential devices: differential drivers are nearly immune to backdrive degradation. Backdriving a differential driver means transposing the levels on the differential output stage, but since differential drivers are current based and use small differential voltages, this presents the drivers with nearly normal conditions.

Degradation mechanism	Expected lifetime degradation
Electromigration	1ms backdrive results in a device lifetime reduction on the order of seconds, tens of seconds
Stress migration	Acceleration factor is orders of magnitude smaller than for electromigration; therefore, stress migration by backdrive not significant
Time dependent dielectric breakdown	Acceleration factor due to backdrive on the same order as stress migration; therefore, lifetime reduction not significant
Hot-carrier injection	Acceleration factor due to backdrive on the same order as stress migration; therefore, lifetime reduction not significant
Bond wire fusing	Catastrophic failure when bond wire fusing current and fusing time are exceeded If multiple outputs are backdriven simultaneously, sum the backdrive currents

Table 3 Expected lifetime degradation

Table 3 summarizes the expected lifetime degradation of an IC exposed to backdrive during an in-circuit test. It should be noted that any given design may incorporate old, new, or a mix of old and new technology. Therefore, it is best to design in-circuit test with both old and new technologies in mind. Fortunately, this is easy to accomplish given that typical ICT design recommendations are valid for both old and new technologies. We can apply the results of original and current research and techniques to our advantage for both mature and modern devices. For example, ensuring good signal quality through fixturing techniques and proper test construction will help to avoid over voltage that may cause CMOS latch-up in older devices as well as help to meet the more demanding margins of low-voltage.

Practical recommendations

Low-voltage

For repeatable testing of low-voltage logic, you must be concerned with not only the test system specifications, but also the DUT characteristics and fixturing. On the Agilent Medalist 3070 and i5000, you can certainly test low-voltage logic devices, but you must be careful in your test and fixture design. Here are some tips to help be successful with low-voltage logic testing on the Agilent Medalist 3070:

- The Agilent Medalist 3070 and i5000 typical specifications are much better than the "guaranteed" specs (+/- 50mV for drivers, +/- 30mV for receivers).
- Set the drive and receive levels to work within the accuracy specifications of the drivers and receivers.
- Make sure to define the appropriate logic families in the 'board' file and reference them in the low-voltage logic libraries (check the 'family' statement in the VCL library).
- Try to disable or condition upstream devices to minimize the backdrive current. This will reduce the inaccuracy caused by the voltage drop due to the output impedance of the driver and other fixture-related impedances.
- Be careful with your slew rate settings to minimize overshoot and undershoot while still meeting the minimum slew rate of the device.
- Use a ground plane with a short-wire fixture or a wireless fixture technology to minimize noise that can cause intermittent tests. Avoid long-wire fixtures as these tend to pick-up more electrical noise.
- Twisted pair, ferrite beads.
- Be diligent in fixture maintenance to minimize probe contact resistance which can cause further driver inaccuracies.

Safeguard

For safe testing of low-voltage devices, continue to use Safeguard by selecting the correct model, including the Agilent updated Safeguard files for modern devices. Also note the overlap between safe testing and repeatable low-voltage testing. For example, minimizing backdrive current helps ensure signal quality as well as minimizing device stress.

- Disable upstream devices whenever possible to avoid backdriving altogether.
- Backdrive a steady state for reliability and reduction of voltage over/undershoot. Set upstream outputs to a fixed logic level by using preconditioning on the 3070 and Agilent Medalist i5000. Select the logic level that requires the least amount of backdrive current – for example backdriving a "1" to a

"0" typically requires less current. This will reduce device stress and potential degradation.

- When in doubt use "default". The existing Safeguard files tend to be conservative for modem devices. If device safety is the primary concern, using Safeguard defaults will generally result in the most conservative analysis. Of course, this could result in a test being inhibited when it need not be. If test coverage is the greater concern, then select the proper Safeguard file to ensure the test would be inhibited only when really necessary.
- Do not use "safeguard none" to turn off Safeguard protection unless the circumstances are well understood. There are times when "safeguard none" is appropriate, but indiscriminate use may set the stage for unacceptable device degradation if not outright damage.
- To remove a Safeguard inhibit: 1) disable upstream devices; or 2) reduce the vector cycle time to reduce the overall test time; or 3) split the test into multiple tests.

Learning backdrive current

Obviously, one of the key external factors of backdrive is current. While backdrive current itself is not the only contributor to device degradation, it is a necessary component of the equation. Backdrive current can be estimated or learned. Product note [1] describes how to perform a theoretical analysis of TTL devices to estimate a worst-case condition. It also describes how to measure actual backdrive current during in-circuit test. In addition, most modern devices have IBIS models ("I/O Buffer Information Specification" [5]) available from which backdrive current can be determined. These techniques can be used to validate the backdrive current entry in the algorithm's models for new devices and device families. As already stated, simply measuring the amount of backdrive current required is not sufficient to determine potential device degradation. Backdrive current, temperature rise, and number of overdriven outputs must all be considered in determining the amount of time a test can run without causing device damage or significant degradation.

Summary

One of the current and continuing challenges facing in-circuit test is the increasing use of low-voltage devices. Driven by miniaturization, the quest for speed, and the conservation of power, IC and board designers are moving towards lower and lower operating voltages. With lower operating voltages come smaller margins and less immunity to noise. With newer devices come renewed concerns regarding the potentially harmful effects of backdrive during in-circuit test.

Obviously a test system's specifications such as driver and receiver accuracy are important. Especially with low-voltage testing, the tester must be able to drive and receive signals within a much smaller margin than in the past. It must be able to cope with the additional demands for signal quality and noise immunity. When the tester can meet the low-voltage margins, a good in-circuit test design needs to include proper fixture design and build. We can see the effects a test fixture can have even on a test system with tight specifications. While care needs to be taken during fixture design and build, techniques used to help ensure signal quality and reduce noise are not new. For example, using the shortest wire possible will help ensure the wanted signal reaches the device under test. Short wires are automatic with the Agilent 3070 and Agilent Medalist i5000.

Another way to gain signal quality is to eliminate backdrive through good DFT practices. We see how higher backdrive current results in additional voltage drop between the tester and DUT. This voltage drop becomes appreciable with lower supply voltages and margins. By avoiding or eliminating backdrive through device disabling, the improved signal quality will increase test reliability.

When backdrive is eliminated, we also reduce or eliminate device stress during in-circuit test. While device degradation due to backdrive is negligible within proper constraints, it is of no concern if devices

are not backdriven. When test reliability and device safety are of concern, good DFT cannot be overemphasized. Device disabling that comes out of DFT not only generally aids signal quality, it also eliminates backdrive induced device stress.

Of course, there will still be times when backdrive is unavoidable. In that case, we need to understand the effects of backdrive and the constraints to safe testing. The primary limit to safe testing is the amount of time a device is in a backdriven condition. Factors contributing to the various degradation mechanisms, and thus the determination of safe test time, include backdrive current, backdrive voltage, power dissipation, temperature, and number of outputs backdriven. Taking all of these items into account, Safeguard In-circuit can predict a maximum test time for a given device under test. If the test time exceeds the maximum safe test time, the test will not be allowed to execute. The predictive nature of Safeguard will not allow inadvertent execution of a test that may lead to device failure or unacceptable device degradation.

Just as in the early days of Safeguard In-circuit, research continues to underscore the Safeguard approach. In fact, for modern devices, existing Safeguard models are typically too conservative. While this provides greater device safety, it can also limit testing of devices that are unnecessarily inhibited. With research again as the foundation, updated logic family definitions and safeguard models will allow test programmers to more accurately match mature and modern device parameters – providing for continued device safety while maximizing test coverage. Fortunately, the Agilent 3070 and Agilent Medalist i5000 test system is already capable of addressing signal quality and safe digital isolation of low-voltage devices. The driver and receiver hardware is able to drive and receive the low-voltage signals. The fixturing techniques help ensure the signal from the test system reaches the device under test as expected. And the Agilent Safeguard In-circuit software continues to protect devices from potential backdrive damage.

Appendix

Updated information for the 3070 and Agilent Medalist i5000

Family definitions

Here are recommended values families for "board_defaults" on the 3070

JEDEC Std Reference [2]	Family	V_{DD}	Part Ref	Drive High	Drive Low	Receive High	Receive Low	Slew	Open Input	Load
No. 8-5	LVCMOS25	2.5 V	AHC, ALVT	2.2	0.1	1.5	0.9			
No. 8-6	LVDIFF15	1.5 V		1.4	0.3	0.9	0.6			
No. 8-7	LVCMOS18	1.8 V	AVC, LVC, ALVC	1.6	0.1	1.2	0.7			
No. 8-B	LVTTL	3.3 V	LV, LVT	2.8	0.2	2.2	0.6			
	LVCMOS	3.0 V	AC	2.6	0.2	2.6	0.4			
No. 8-11	LVCMOS15	1.5 V	AVC	1.4	0.0	0.9	0.6			
No. 8-12	LVCMOS12	1.2 V	AVC, AUC	1.1	0.0	0.7	0.5			
No. 8-14	LVCMOS10	1.0 V	AUC	0.9	0.0	0.6	0.5			

Here are recommended values families for "board_defaults" on the Medalist i5000

JEDEC Std Reference [2]	Family	V_{DD}	Part Ref	Drive High	Drive Low	Receive	Open Input	Load
No. 8-5	LVCMOS25	2.5 V	AHC, ALVT	2.2	0.1			
No. 8-6	LVDIFF15	1.5 V		1.4	0.3			
No. 8-7	LVCMOS18	1.8 V	AVC, LVC, ALVC	1.6	0.1			
No. 8-B	LVTTL	3.3 V	LV, LVT	2.8	0.2			
	LVCMOS	3.0 V	AC	2.6	0.2			
No. 8-11	LVCMOS15	1.5 V	AVC	1.4	0.0			
No. 8-12	LVCMOS12	1.2 V	AVC, AUC	1.1	0.0			
No. 8-14	LVCMOS10	1.0 V	AUC	0.9	0.0			

Safeguard files

Table 4 includes some typical backdrive currents from devices sampled by 0. Vo is the overdrive voltage that is in this case equal to Vcc. This approach is somewhat conservative in that drive levels are typically below Vcc; therefore, Vo would be somewhat less than Vcc. Of course this distinction diminishes, as Vcc gets smaller with lower voltage devices. I("0") is the amount of current required to overdrive a logic "1" to a logic "0" level.

Family	Vcc	Vo	Backdrive current I("0")	Backdrive current I("1")
CMOS				
HC	5	5	68 mA	60 mA
AC	3.3 - 5	5	232 mA	203 mA
AHC	2.2 - 5	5	70 mA	66 mA
LV	3.3 - 5	5	165 mA	123 mA
LVC	1.8 - 3.3	3.3	100 mA	112 mA
ALVC	1.8 - 3.3	3.3	137 mA	236 mA
AVC	1.2 - 3.3	3.3	182 mA	232 mA
BiCMOS				
F	5	5	72 mA	611 mA
BCT	5	5	150 mA	723 mA
ABT	5	5	173 mA	295 mA
LVT	2.8 - 3.3	3.3	165 mA	270 mA
ALVT	2.5 - 3.3	3.3	196 mA	235 mA

Table 4 Typical backdrive current

Agilent 3070 and Medalist i5000 comparison chart

A comparison chart between the Agilent 3070 and Agilent Medalist i5000 showing the key specifications related to low voltage testing is shown in Table 5.

Feature	Agilent 3070	Agilent Medalist i5000
Driver output impedance	1.15-2.0 ohms	0.87 ohms (typical)
Driver output accuracy	+/- 50mV typical, +/-100mV guaranteed	+/- 50mV
Receiver input voltage accuracy	+/- 30mV typical, +/-100mV guaranteed	+/-30mV typical, +/-100mV guaranteed
Driver and Receiver programming resolution	2.2mV	20mV
Driver output voltage range	-3.0V to +5.0V	0.0V to 5.0V
Slew rate	25V/uS to 250V/uS	Fixed 300V/uS

Table 5 Comparison of key specifications between Agilent Medalist 3070 and i5000.

References

[1] Safeguard In-Circuit, Hewlett-Packard Product Note 3065-2, 1985.

http://www.agilent.com/see/pcb

[2] Failure Mechanisms and Models for Semiconductor Devices, JEDEC Publication JEP122B, 2003.

http://www.jedec.org/Catalog/display.cfm

[3] Ugur Cilingiroglu, Backdrive Damage Mechanisms in Modern Integrated Circuits, 2003.

http://www.agilent.com/see/pcb

[4] A.J. Albee, The Challenges of Testing Low Voltage Devices at In-circuit Test. TUG 2003.

http://www.teradyne.com/atd/resource/type/technical_papers.html

[5] IBIS (I/O Buffer Information Specification) ANSI/EIA-656-A

http://www.eigroup.org/IBIS

Printed in USA April 19, 2005

Agilent Technologies